Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OSC-OUT**
2. **XTAL-5**
3. **XTAL-10**
4. **OEL**
5. **OEH**
6. **OSC-L01**
7. **GND**
8. **OUT**
9. **VCC**
10. **TRF**
11. **DIVA**
12. **OSC DR**
13. **DIVB**
14. **GNDQ**
15. **DIVBB**
16. **OSC IN**
17. **XTAL-20**

**.062”**

**MASK**

**REF**

**2 1 18 17 16 15**

**3**

**4**

**5**

**6**

**7 8 9 10**

**14**

**13**

**12**

**11**

**J3301Z**

**.062”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Vcc**

**Mask Ref: J3301Z**

**APPROVED BY: DK DIE SIZE .062” X .062” DATE: 8/30/22**

**MFG: NATIONAL/FSC THICKNESS .015” P/N: 54ACT3301**

**DG 10.1.2**

#### Rev B, 7/1